Hall Ticket Number:

Code No. : 18431 (B) N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) VIII-Semester Main & Backlog Examinations, May-2023

Low Power VLSI Design (PE-V)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	What is the need of low power VLSI design?	2	1	1	1	1
2.	In the CMOS circuit, if the frequency is doubled, supply voltage is made half, capacitance is increased 4 times, dynamic power will increase by how many times?	2	1	2	2	1
3.	Write an expression for threshold voltage of MOSFET considering body effect	2	3	1	2	1
4.	What are the expressions for drain current in non-saturated and saturated regions?	2	3	1	2	1
5.	Mention dynamic power consumption components of CMOS inverter	2	1	3	1	1
6.	List various types of circuit technology independent and dependent power reduction techniques.	2	1	3	1	1
7.	Give various circuit techniques to reduce leakage in cache memories.	2	1	4	2	1
8.	What is the effect of low oxide thickness in MOSFET?	2	1	4	2	1
9.	State the advantages and disadvantages of carry look ahead adder?	2	1	5	2	1
10.	Mention the advantages of logarithmic adders.	2	1	5	1	1
	Part-B (5 × 8 = 40 Marks)					
11. a)	Explain about hot carrier effects in MOSFETS.	4	2	1	1	1
b)	Describe about different types of MOS Capacitances.	4	2	1	1	1
12. a)	Explain about narrow channel effects in MOSFETS.	5	2	2	1	1
b)	Define sub-threshold current and write the expressions for it.	3	2	2	2	1
13. a)	Explain circuit parallelization technique with the help of an example	5	3	3	2	1
b)	Describe multiple voltages technique with the help of an example	3	3	3	2	1

Contd... 2

14. a)	Describe dual threshold CMOS technique with a circuit diagram	3	2	4	2	1
b)	Explain about leakage control using transistor stacks technique.	5	2	4	3	1
15. a)	Draw the circuit and explain the working of Carry select adder.	4	3	5	2	1
b)	Compare carry select and carry skip adders	4	3	5	2	1
16. a)	What are the various low power techniques which can be used at RTL, Gate level and circuit level?	4	2	2	2	1
b)	Draw the circuit of BiCMOS inverter and compare it with CMOS inverter.	4	3	1	3	1
17.	Answer any ***two*** of the following:					
a)	Explain retiming technique to reduce independent power with an example	4	3	3	2	1
b)	Describe about dynamic V_{TH} scaling technique.	4	2	4	2	1
c)	Draw the circuit of 28-Transistor Full adder and compare it with other 1-bit full adders.	4	3	5	3	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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